LW 4x/2x/1x FC SFP with DDM

Features

- International Class 1 laser safety certified
- RoHS directive compliant (lead-free)
- 4x,2x,1x (ANSI) Fibre Channel [1] compliant
- Gigabit Ethernet Compatible
- Long wavelength (LW)
- JSH-42L3AD3-5 max. distance of 5 km
- JSH-42L3AD3-20 max. distance of 20 km
- Digital Diagnostic Monitoring Interface SFF-8472 Compliant [5]
- EMI Emissions below Class B
- Single +3.3 V Power Supply
- -15°C ambient to 85°C case operation
- UL and CSA approved
- Optional interrupt on alarms and warnings

Applications

- Fibre Channel
- Ethernet Networking
- Client/Server environments
- Distributed multi-processing
- Fault tolerant applications
- Visualization, real-time video, collaboration
- Channel extenders, data storage, archiving
- Data acquisition

Description

These JDSU SFPs are integrated fiber optic transceivers that provide a high-speed serial link at a signaling rate up to 4.25 Gb/s. They conform to the American National Standards Institute's (ANSI) Fibre Channel, and SFF-8472 specifications.

The JSH-42L3AD3-5 supports a maximum fiber distance of 5 km and is available with blue color identification or gray color identificaiton (JSH-42L3AD3-5G). The JSH-42L3AD3-20 supports a maximum fiber distance of 20 km. These transceivers operate on singlemode fiber only.

The transceiver is ideally suited for Fibre Channel applications which include point to point links as well as Fibre Channel Arbitrated Loop (FC-AL). It can also be used for other serial applications where high data rates are required. This specification applies to a hot-pluggable (SFP) module which is an electrical surface-mount connector assembly.

The transceiver features a microprocessor with imbedded non-volatile RAM. Vital product data is stored in the NVRAM and several optical and electrical characteristics of the transceiver are computed "Real-Time" with the results written to memory. This data can all be accessed by a two-wire serial interface at the SFP connector.

Encoded (8B/10B) [3], [4], serial differential signals traverse the connector interfacing the transceiver to the host card. The serial data modulates the laser and is sent out over the outgoing fiber of a duplex cable.

The transceiver is a certified Class 1 laser safe product. The optical power levels, under normal operation, are at eye safe levels. Optical fiber cables can be connected and disconnected without shutting off the laser transmitter.

The transceiver is also compliant with the RoHS Directive from the European Union - Directive 2002/95/EC on the Restriction Of use of certain Hazardous Substances. The largest change with optical transceivers comes with the removal of all lead-based parts and soldering. Now it is a lead-free part.

Package Outline

Pin Definitions

Pin #	Pin Name	Type	Sequence	Pin #	Pin Name	Type	Sequence
1	Tx Ground	Ground	1	11	Rx Ground	Ground	1
2	Tx_Fault	Signal Out	3	12	-Rx_DAT	Data Out	3
3	Tx_Disable	Signal In	3	13	+Rx_DAT	Data Out	3
4	MOD_DEF(2)	Input/Output	3	14	Rx Ground	Ground	1
5	MOD_DEF(1)	Input/Output	3	15	Rx Power	Power	2
6	MOD_DEF(0)	Input/Output	3	16	Tx Power	Power	2
7	Reserved	Signal In	3	17	Tx Ground	Ground	1
8	Rx_LOS	Signal Out	3	18	+Tx_DAT	Data In	3
9	Reserved	Signal In	3	19	-Tx_DAT	Data In	3
10	Rx Ground	Ground	1	20	Tx Ground	Ground	1

Laser Safety Compliance

The JDSU transceiver is a CLASS 1 LASER PRODUCT as defined by the international standard IEC 60825-1, Am.2 (2001). The product also complies with U.S.A. regulations for Class 1 products contained in 21 CFR 1040.10 and 1040.11. Laser emissions from Class 1 laser products are not considered hazardous when operated according to product specifications. Operating the product with a power supply voltage exceeding 5.0 volts may compromise the reliability of the product, and could result in laser emissions exceeding Class 1 limits identified in IEC 60825-1, Am.2 (2001); under these circumstances, viewing the transmitter port with optical aides (i.e., eye loupes) should be avoided.

ESD Notice

It is advised that normal static precautions be taken in the handling and assembly of the transceiver to prevent damage and/or degradation which may be introduced by electrostatic discharge.

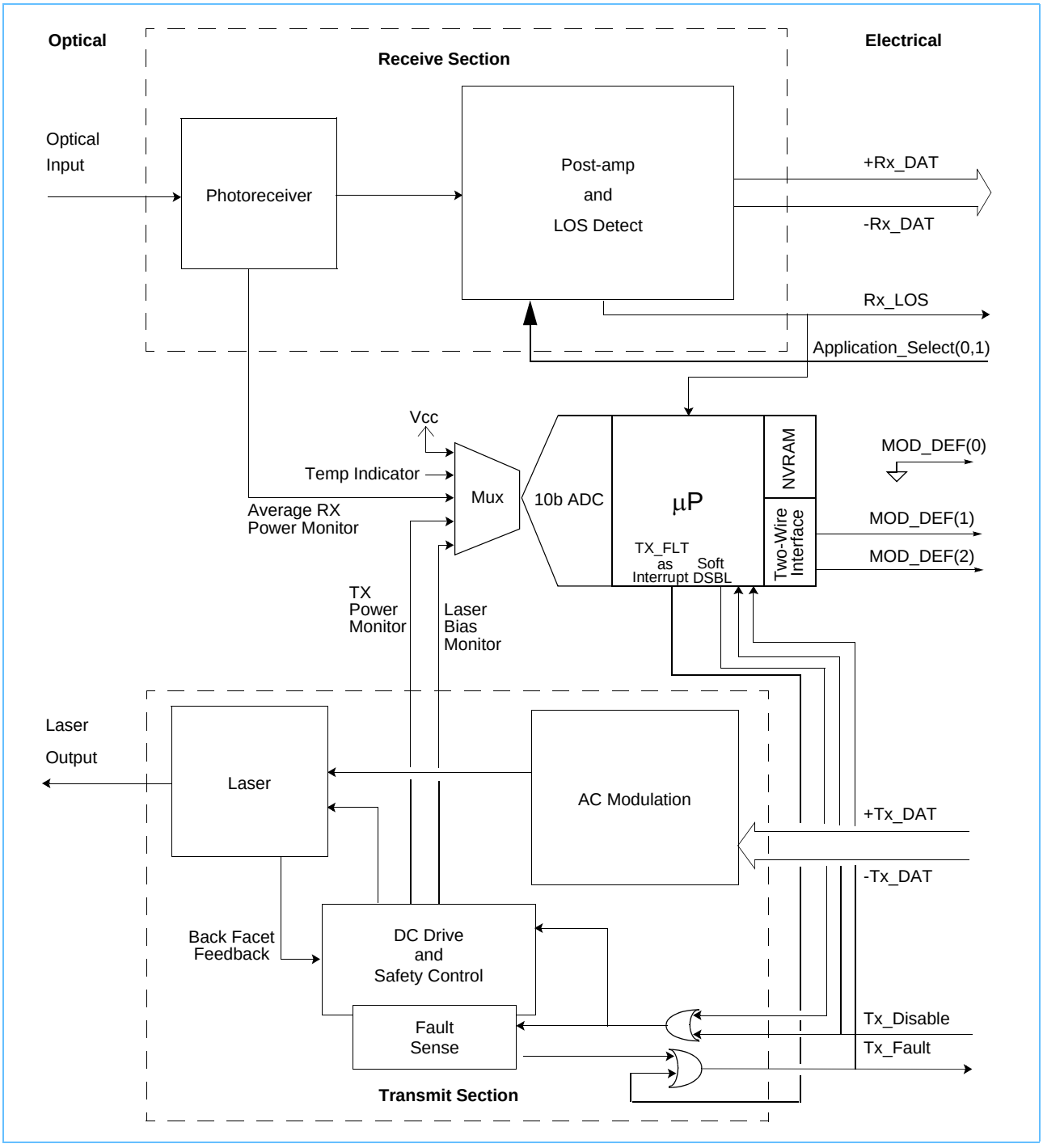
Ordering Information

Part Number[1]	Signaling Rate	Wavelength	Distance Supported[2]	Laser Type
JSH-42L3AD3-5	1.0625 Gb/s, 2.125 Gb/s, or 4.25 Gb/s	1310 nm	5 km	FP (Fabry-Perot)
JSH-42L3AD3-5G	1.0625 Gb/s, 2.125 Gb/s, or 4.25 Gb/s	1310 nm	5 km	FP (Fabry-Perot)
JSH-42L3AD3-20	1.0625 Gb/s, 2.125 Gb/s, or 4.25 Gb/s	1310 nm	20 km	DFB (Distributed Feedback)

1. All transceivers come with a Blue bail cover, except those that end with a "5G". "5G" come with a Gray bail cover.

2. When used with two JDSU transceivers.

Block Diagram



Transmit Section

The input, an AC coupled differential data stream from the host, enters the AC Modulation section of the laser driver circuitry where it modulates the output optical intensity of a semiconductor laser. The DC Drive circuit incorporates an automatic power control (APC) loop which maintains the laser at the correct preset power level. In addition, safety circuits in the DC Drive will shut off the laser, or guarantee safe launch power if a fault is detected. *The transceiver provides the AC coupling for the +Tx/-Tx lines.* No AC coupling capacitors are required on the host card for proper operation. There are two outputs from the transmitter section that deliver signals proportional to the average transmitted optical power and also the laser average bias current. These signals are digitized and processed within the transceiver for the Digital Diagnostic Monitoring feature.

Receive Section

The incoming modulated optical signal is converted to an electrical signal by the photoreceiver. This electrical signal is then amplified and converted to a differential serial output data stream and delivered to the host. A signal strength detector indicates whether light is present or not at the input to the photoreceiver. This signal is provided to the host as a loss-of-signal (Rx_LOS) status line. *The transceiver provides the AC coupling for the +Rx/-Rx lines.* No AC coupling capacitors are required on the host card for proper operation. There is an output from the pre-amplifier in the photoreceiver that is proportional to the average optical power incident on the photodiode. This signal is digitized and processed within the transceiver as part of the Digital Diagnostic Monitoring feature.

Digital Diagnostic Monitoring

The digital diagnostic monitoring feature is compliant with document SFF-8472, “Digital Diagnostic Monitoring Interface for Optical Transceivers” [5]. In addition to transmitted optical power, laser-bias current and received optical power, there are also sensors for transceiver temperature and supply voltage which are all multiplexed to the analog-to-digital converter. After the signals are digitized, they are processed and compared to alarm levels for the optional alarm features and interrupts. The real-time values of each monitored parameter can be read and used for evaluating the status of the link. Also, the alarm/warning bits can be used to provide transceiver status or enable an interrupt notification. A user-writable non-volatile RAM scratch space for customer use is limited to 100,000 write cycles.

Optional Monitor TX_FAULT Alarm/Warning Interrupt

The transceiver provides programmable Alarm/Warning Interrupt Enable bits. They are used by the transceiver to generate a TX_FAULT signal usable as an interrupt to the host for an alarm/warning condition. This is an extension to the polling architecture of SFF-8472 and allows for interrupt driven host microcode. For a complete description see section “Vendor Specific Digital Diagnostic Monitor TX_FAULT Alarm/Warning Interrupt” on page 37.

Input Signal Definitions

Levels for the signals described in this section are listed in Transmit Signal Interface on page 16 and Control Electrical Interface on page 17.

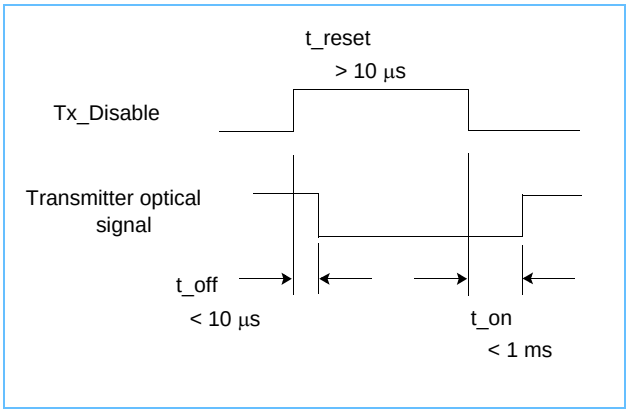
Tx_DAT

A differential serial data stream is presented to the transceiver for transmission onto an optical fiber by modulating the optical output intensity of the laser.

Tx_Disable

When high (logic one), the Tx_Disable signal turns off the power to both the AC and DC laser driver circuits. It will also reset a laser fault if one should happen. When low (logic zero), the laser will be turned on within 1ms unless a Tx_Fault condition exists.

When this signal is asserted, the laser monitoring function will report low power and low bias current. The alarm/warning flags for these quantities will also become active. Additionally, the Tx_Disable indicator, bit 7 in byte 110 of the DDM page will become active. See Monitor Data Table 4 on page 35.



Application_Select (0:1)

The transceiver provides multiple application selection capability in accordance with the SFF-8079+ and SFF-8089[6]. The Application_Select pins control internal settings which configure the transceiver for optimal performance at a given data rate. The Application_Select(0) was previously labelled Rate Select and Application_Select(1) was an Rx Ground. Full software control based on the application select tables in the A0 page is also available. These pins are compatible with previous implementations of SFP transceivers.

Data Rate	4xFC (4.250 Gb/s)	2xFC (2.125 Gb/s)	1xFC (1.0625 Gb/s)	**GbE (1.250 Gb/s)**
Application_Select(0)	0 or 1 or float	0 or 1 or float	0 or 1 or float	Not applicable
Application_Select(1)	0 or 1 or float	0 or 1 or float	0 or 1 or float	Not Applicable

Output Signal Definitions

Levels for the signals described in this section are listed in Receive Signal Interface (from transceiver to host) on page 17 and Control Electrical Interface on page 17.

Rx_DAT

The incoming optical signal is converted and repowered as a differential serial data stream. The Receive Signal Interface (from transceiver to host) table on page 17 gives the voltage levels and timing characteristics for the Rx_DAT signals.

Rx_LOS

The Receive Loss of Signal line is high (logic one) when the incoming modulated light intensity is below that required to guarantee the correct operation of the link. Normally, this only occurs when either the link is unplugged or the companion transceiver is turned off. This signal is normally used by the system for diagnostic purposes.

This signal has an open drain TTL driver. A pull up resistor is required on the host side of the SFF connector. The recommended value for this resistor is 10 kΩ.

Tx_Fault

Upon sensing an improper power level in the laser or any other potentially unsafe condition, the SFF sets this signal high and turns off the laser. The Tx_Fault signal can be reset with the Tx_Disable line.

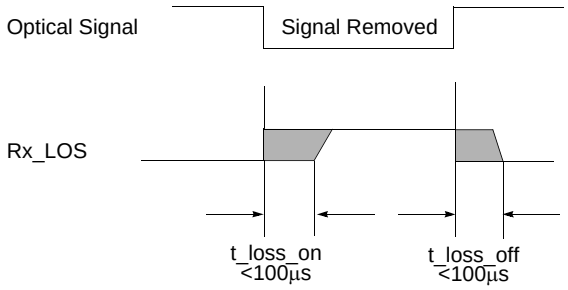
The laser is turned off within 100 μs as shown in the Transmitter Fault Detection timing diagram below.

This signal has an open drain TTL driver. A pull up resistor is required on the host side of the SFF connector. The recommended value for this resistor is 10 kΩ.

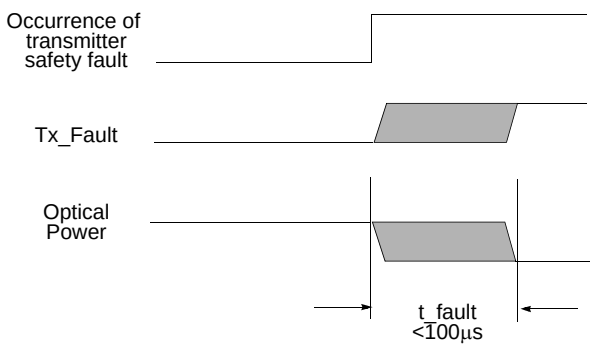
Tx_Fault can also become active if the alarm/warning enable control bits are set within the 0xA2page. For a complete description see section “Vendor Specific Digital Diagnostic Monitor TX_FAULT Alarm/Warning Interrupt” on page 37.

Output Signal Timings

Receive Loss of Signal Detection



Transmitter Fault Detection



MOD_DEF(0:2)

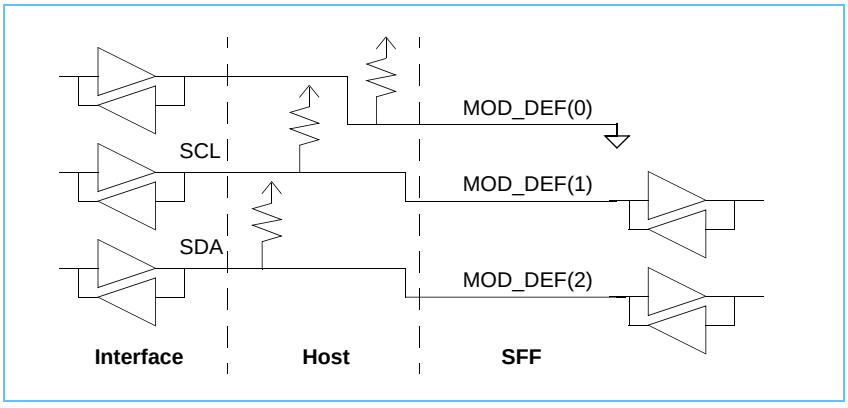
A two-wire serial interface is used to access two 256-byte memory spaces that describe some of the capabilities, standard interfaces, manufacturer, optical monitor levels, alarms and other information relevant to the product. Some of this space is protected and some is user writable. Also some of the space is non-volatile so that information is retained during unpowered conditions. Tables describing the specific addresses and values of the memory space are included in Two-Wire Interface Timing Specifications on page 23 and on page 31. Operation of the two-wire interface is described in Two-Wire Protocol for Serial ID and Digital Diagnostic Monitoring Information on page 11. Signal timings necessary for proper operation of the Serial ID function are shown in Two-Wire Interface Timing Specifications on page 23.

The two-wire interface requires both a serial clock (SCL) and serial data I/O (SDA) connections. These signals are required to have pull up resistors on the host board to the 3.3V supplying the transceiver (4.7 kΩ is the recommended value; however, a smaller value may be needed in order to meet the Serial ID's rise and fall time requirements). The following list and figure show the necessary connections from an interface to a SFF to ensure the capability of reading the Serial ID data.

MOD_DEF(0): Logic Low
MOD_DEF(1): SCL
MOD_DEF(2): SDA

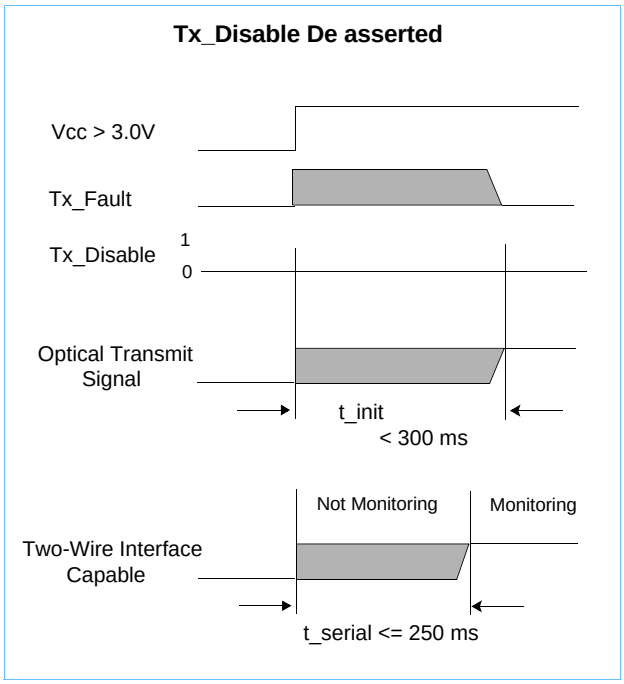
The serial clock (SCL) and the serial data (SDA) lines appear as NC to the host system upon initial power up.

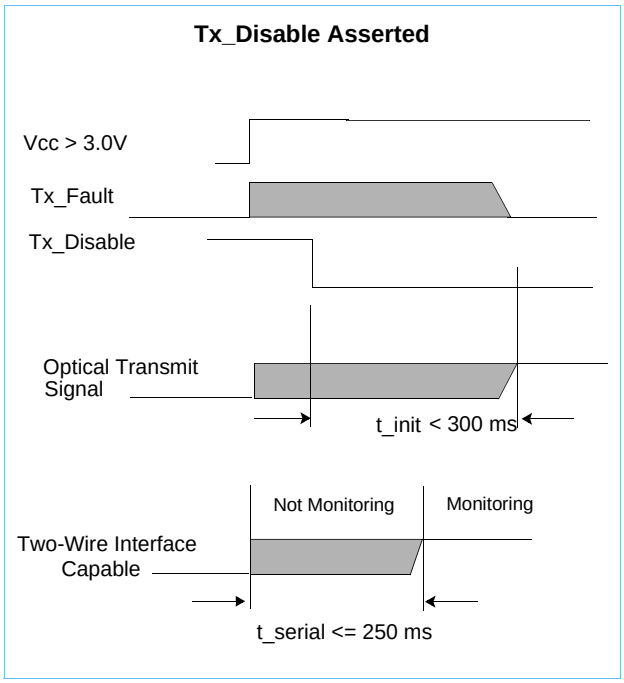
Expected Connections to SFF MOD_DEF Pins



Operation

Initialization Timings





Two-Wire Interface Capable

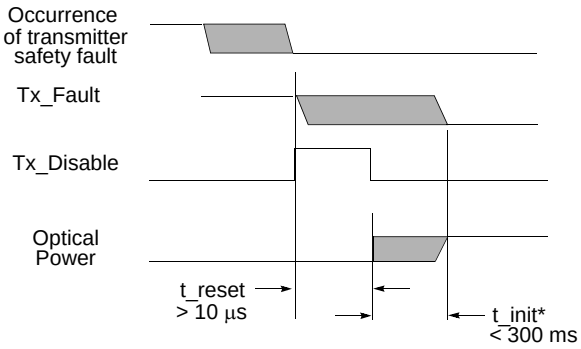
The transceiver will be capable of responding to a start sequence on the Two-Wire interface (see “Two-Wire Protocol for Serial ID and Digital Diagnostic Monitoring Information” on page 11) 250 ms after application of 3.0 volts, or greater up to maximum, at the voltage inputs of the transceiver. If a start sequence is transmitted by the host prior to 250 ms after power is good, the transceiver may not acknowledge the sequence.

Resetting a Laser Fault

Resetting a laser fault by toggling the Tx_Disable input will permit the transceiver to attempt to power on the laser following a fault condition.

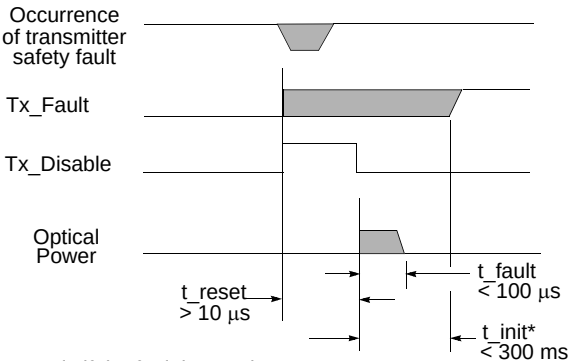
Fault Condition Recovery Timings

Successful Recovery from a Transmitter Safety Fault



*only if the fault is transient

Unsuccessful Recovery from a Transmitter Safety Fault



*only if the fault is transient

Two-Wire Protocol for Serial ID and Digital Diagnostic Monitoring Information

Product specific information is stored in the device and is accessible via a standard two-wire interface. Some of the data is non-volatile and some is updated real time with data that characterizes critical conditions of the transceiver. While most registers are read only, some registers can be written by the customer for use as scratch space or to set interrupt enables or clear interrupt indicators.

There are two data addresses which can be used to access two different sets of data. The page address 0b1010000X is used for the set of Serial ID data and the page address 0b1010001X is used for the set of Digital Diagnostic Monitoring information.

Critical timings for communicating to the module on the two-wire interface are shown in Two-Wire Interface Figure 8 on page 14. For more information on the Serial ID protocol, see Two-Wire Interface Timing Specifications on page 23.

Two-wire Data Read

To read data from the device, the following sequence must occur on the Two-wire interface (refer to Two-Wire Interface Figure 2 on page 13, Two-Wire Interface Figure 3 on page 13, and Two-Wire Interface Figure 4 on page 13 throughout these steps):

1. Send a start signal to the module.

   A start signal is presented by toggling the data line from high to low while the clock is high (see Two-Wire Interface Figure 2 on page 13).

2. Send the write data sequence.

   The write data sequence consists of the bits 0b10100000 for the Serial ID data or 0b10100010 for the Digital Diagnostic Monitoring information.

3. Receive an acknowledge signal.

   One zero bit is the acknowledge signal.

   Once this sequence has been acknowledged, the user will send the memory address to start reading from.

4. Send the address of the first byte to be read during the subsequent sequence.
5. Receive an acknowledge signal.
6. Send a start signal.
7. Send the read data sequence.

   The read data sequence consists of the bits 0b10100001 for the Serial ID data or 0b10100011 for the Digital Diagnostic Monitoring information.

8. Receive an acknowledge signal.

   Once this sequence has acknowledged, the user will begin receiving data bytes.

9. Receive a data byte.
10. Send an acknowledge signal to receive the next, consecutive data byte, or send a no-acknowledge signal followed by a stop signal to stop receiving data.

    A stop signal is presented by toggling the data line from low to high while the clock is high (see Two-Wire Interface Figure 2 on page 13).

Two-wire Data Write

To write data to the Digital Diagnostic Monitoring data address of the device (writes are not allowed to the Serial ID data address), the following sequence must occur on the Two-wire interface (refer to Two-Wire Interface Figure 1 on page 13, Two-Wire Interface Figure 2 on page 13, and Two-Wire Interface Figure 3 on page 13 throughout these steps):

1. Send a start signal to the module.

   A start signal is presented by toggling the data line from high to low while the clock is high (see Two-Wire Interface Figure 2 on page 13).

2. Send the data write sequence.

   The write data sequence consists of the bits 0b10100000 for the Serial ID data or 0b10100010 for the Digital Diagnostic Monitoring information.

3. Receive an acknowledge signal.

   One zero bit is the acknowledge signal.

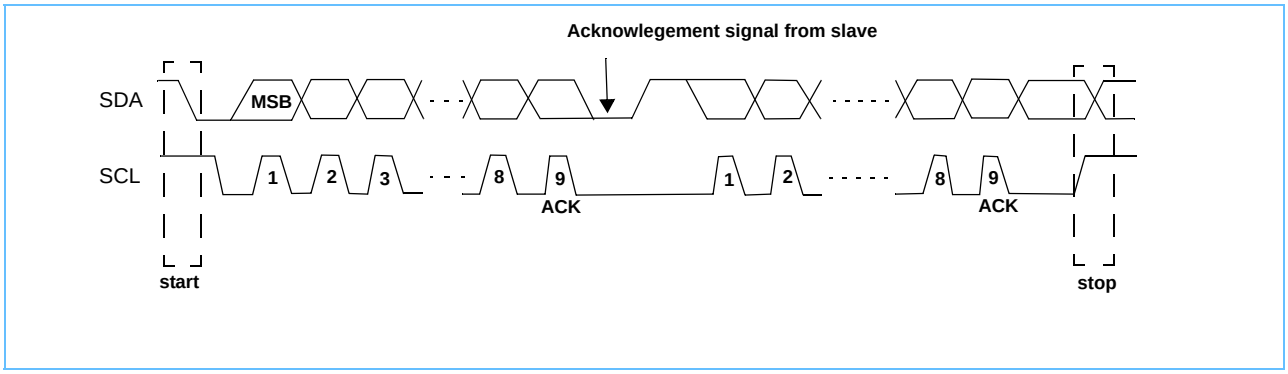
4. Send the address of the first byte to be written during the subsequent sequence.

   Valid byte addresses are 0b01101110 for one byte, and byte addresses 0b10000000 thorough 0b11110111.

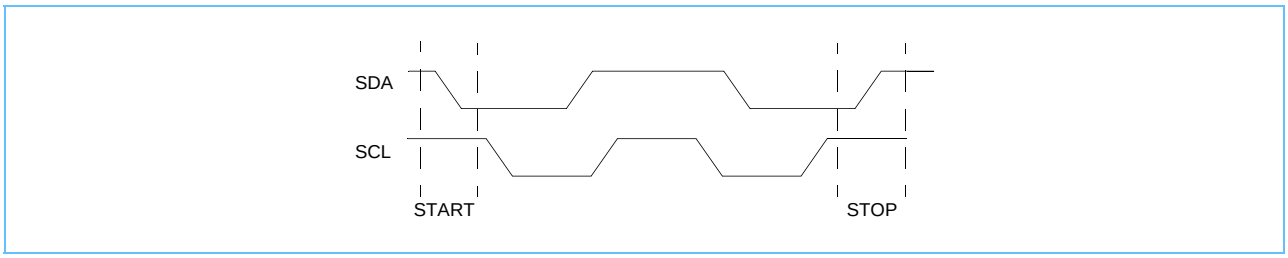
5. Receive an acknowledge signal.
6. Send a data byte.
7. Receive an acknowledge signal.
8. Send the next, consecutive data byte (reference Two-Wire Interface Figure 7 on page 14), or send a stop signal to stop sending data (reference Two-Wire Interface Figure 6 on page 14).

A stop signal is presented by toggling the data line from low to high while the clock is high (see Two-Wire Interface Figure 2 on page 13).

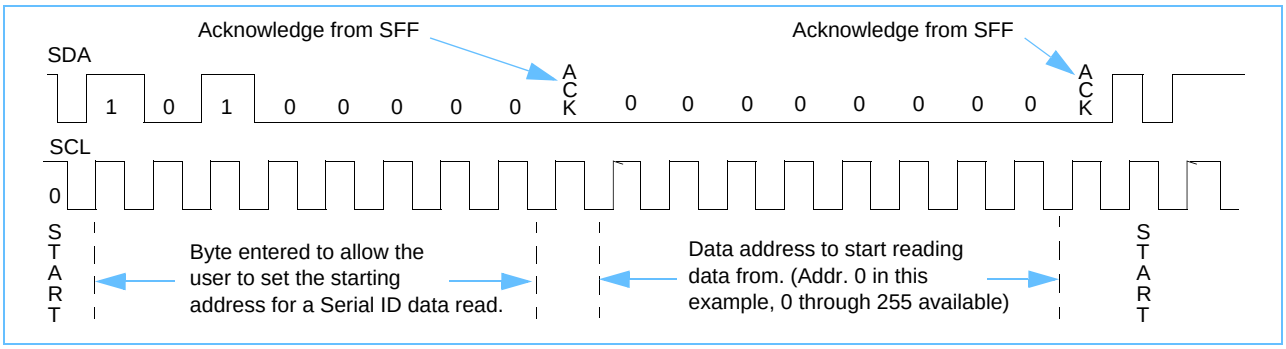
Two-Wire Interface Figure 1 Data transfer on the Two-wire interface



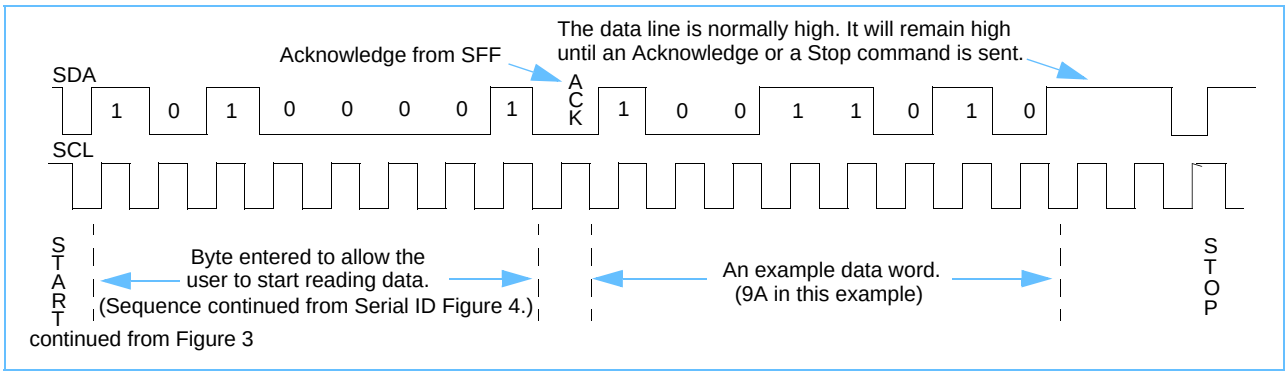
Two-Wire Interface Figure 2 Start and Stop TIming



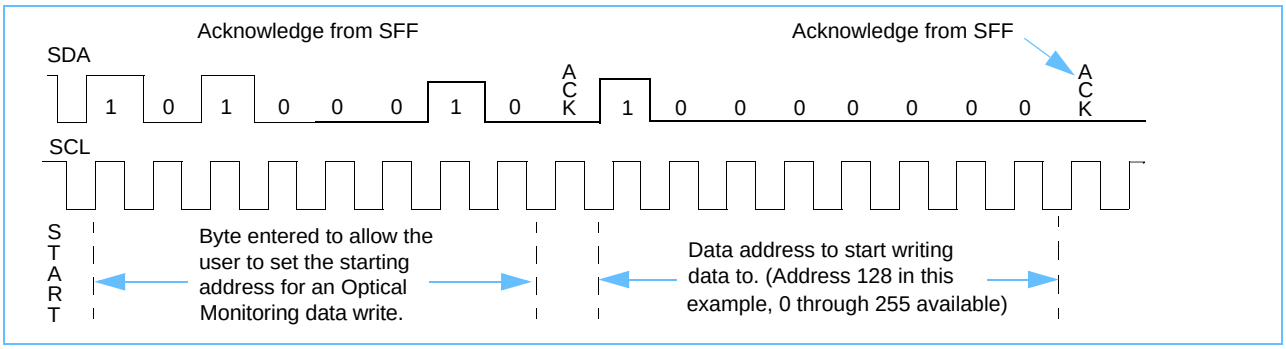
Two-Wire Interface Figure 3 Set Data Address Sequence for Read Timing



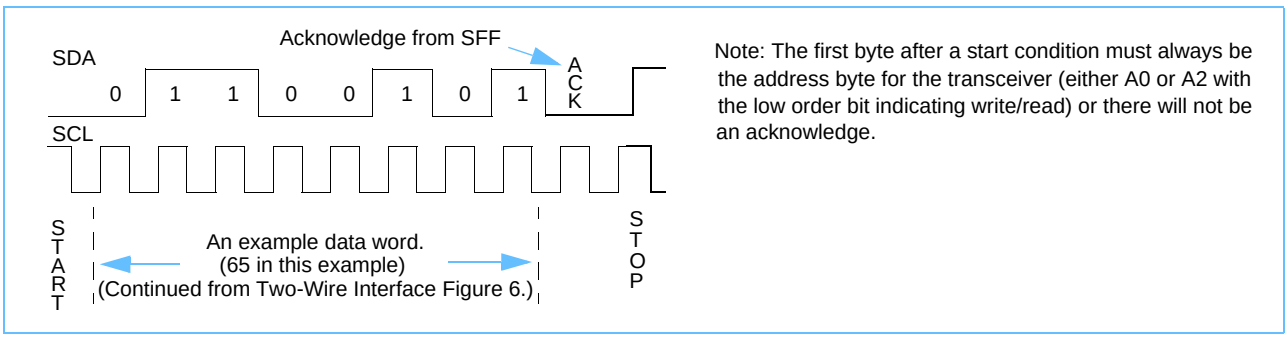
Two-Wire Interface Figure 4 Read Data Sequence Timing



Two-Wire Interface Figure 5 Set Data Address Sequence for Write Timing

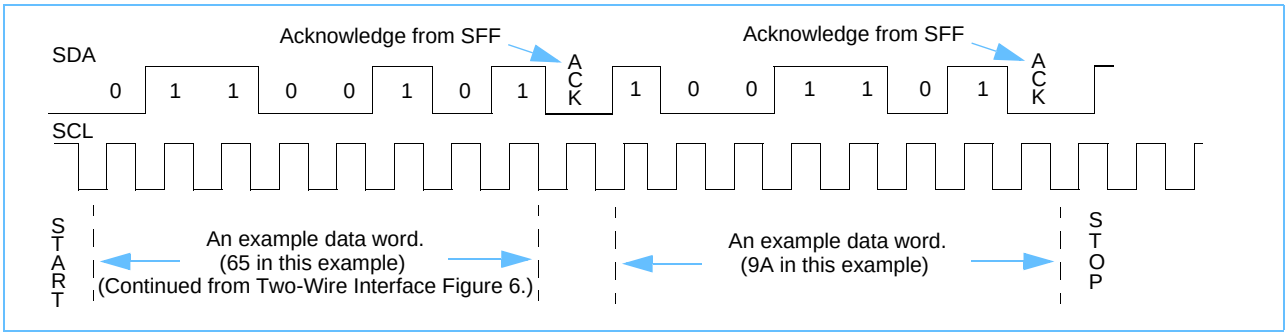


Two-Wire Interface Figure 6 Write Data (Single-Byte) Sequence Timing

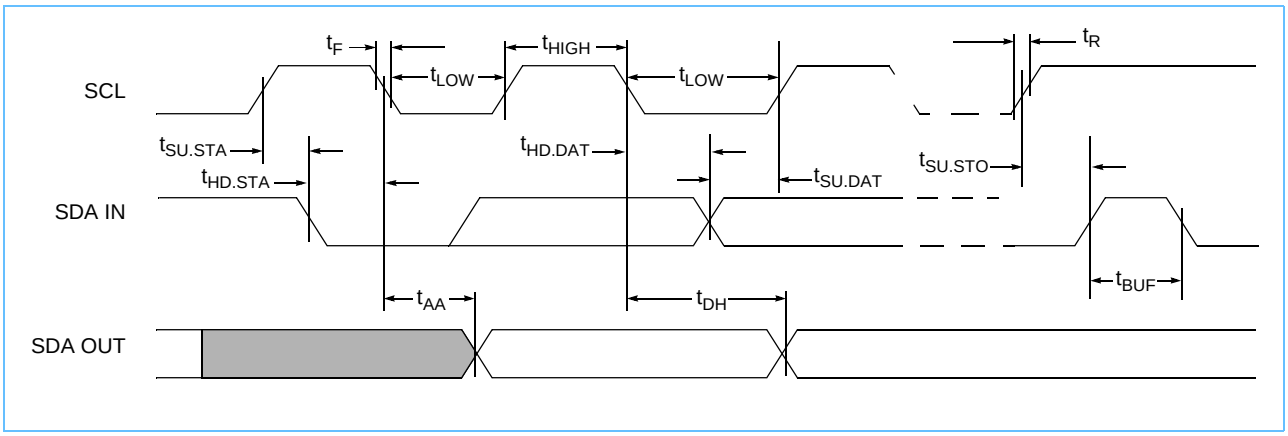


Note: The first byte after a start condition must always be the address byte for the transceiver (either A0 or A2 with the low order bit indicating write/read) or there will not be an acknowledge.

Two-Wire Interface Figure 7 Write Data (Multi-Byte) Sequence Timing



Two-Wire Interface Figure 8 Critical Timings
Parameters are defined in Two-Wire Interface Timing Specifications on page 23.



Absolute Maximum Ratings

Symbol	Parameter	Min.	Typical	Max.	Unit	Notes
T_S	Storage Temperature	-40		85	°C	1
RH_S	Relative Humidity–Storage	0		90	%	1, 2
V_{CC}	Supply Voltage	-0.5		5.0	V	1
V_I	TTL DC Input Voltage	0		V_{CC} + 0.7	V	1
	Non-Volatile Write Cycles			100,000	cycles	

1. Stresses listed may be applied one at a time without causing permanent damage. Exposure to these values for extended periods may affect reliability. Specification Compliance is only defined within Specified Operating Conditions.
2. Non-condensing environment.

Specified Operating Conditions

Symbol	Parameter	Min.	Typical	Max.	Unit
T_{OP}	Operating Temperature	-15		85[1]	°C
T_{OP}	Operating Temperature[2]	-40		-15	°C
V_{CC}	Supply Voltage (+/- 10%)	3.0	3.3	3.6	V
RH_{OP}	Relative Humidity-Operating	5		90	%

1. Case temperature
2. Compatible operation (BER<10^{-12})

Power Supply Interface

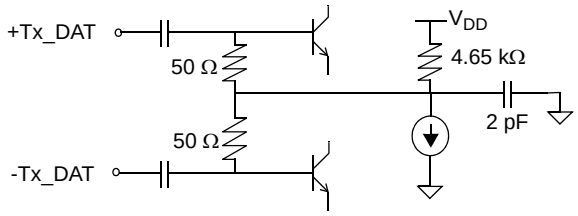
Symbol	Parameter	Min	Typical	Max.	Unit
I_{VCC}	V_{CC} Current (combined Tx and Rx) JSH-42L3AD3-20		200	300	mA
I_{VCC}	V_{CC} Current (combined Tx and Rx) JSH-42L3AD3-5		240	300	mA
P	Total Power Dissipation (combined Tx and Rx) JSH-42L3AD3-20		650	1000[1]	mW
P	Total Power Dissipation (combined Tx and Rx) JSH-42L3AD3-5		800	1000[2]	mW
	Ripple & Noise			100	mV (pk-pk)

1. At 3.3 volts
2. At 3.3 volts

Transmit Signal Interface (from host to transceiver)

Symbol	Parameter	Min	Max.	Unit	Notes
V_o	Amplitude	300	2400	mV	1
$DJ_{elec-xmit}$	Deterministic Jitter		0.14	UI	2
$TJ_{elec-xmt}$	Total Jitter		0.26	UI	2
	Rise/Fall	60		ps	3
	Differential Skew		20	ps	
	Input Return Loss		-11	dB	4
SDD_{11}	Return Loss		-9	dB	4

1. At 100Ω, differential peak-to-peak, the figure below shows the simplified circuit schematic for the transceiver high-speed differential input lines. The input data lines have AC coupling capacitors. The capacitors are not required on the host card.

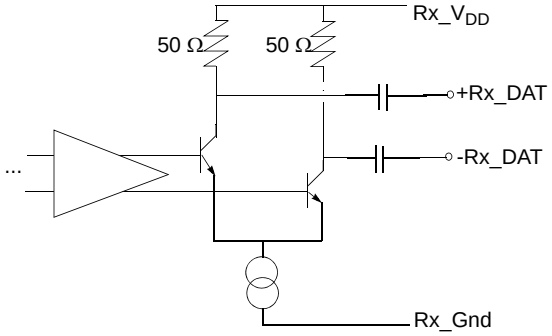


2. Deterministic jitter (DJ) and total jitter (TJ) values are measured according to the methods defined in [2]. Jitter values at the output of a transmitter or receiver section assume worst case jitter values at its respective input. [1UI(Unit Interval)=235.3 ps at 4.25Gb/s]
3. Rise and fall times are measured from 20 - 80%, 100Ω differential.
4. At 2.125 GHz

Receive Signal Interface (from transceiver to host)

Symbol	Parameter	Min	Max.	Unit	Note(s)
V_o	Amplitude	600	1600	mV	1,2
$DJ_{elec-rcv}$	Deterministic Jitter		0.39	UI	3
$TJ_{elec-rcv}$	Total Jitter		0.64	UI	3
	Common Mode Voltage (rms)		30	mV	
SDD_{22}	Return Loss		-9	dB	4
SCC_{22}	Return Loss		-7	dB	4

1. At 100Ω, differential peak-to-peak, the figure below shows the simplified circuit schematic for the transceiver high-speed differential output lines. The output data lines have AC coupling capacitors. The capacitors are not required on the host card.



2. 600 mV Min for "AD3" part numbers.
3. Deterministic jitter (DJ) and total jitter (TJ) values are measured according to the methods defined in [2]. Jitter values at the output of a transmitter or receiver section assume worst case jitter values at its respective input. [1UI(Unit Interval)=235.3 ps at 4.25Gb/s].
4. at 2.125 GHz

Control Electrical Interface

Symbol	Parameter	Min	Max.	Unit	Note(s)
Voltage Levels					
V_{OL}	TTL Output (from transceiver)	0.0	0.50	V	1
V_{OH}		V_{DD} - 0.5	V_{DD} + 0.3	V	
V_{IL}	TTL Input (to transceiver)	0.0	0.8	V	2
V_{IH}		2.0	V_{DD} + 0.3	V	
V_{IL}	Serial ID SCL and SDA lines	0.0	V_{DD} x 0.3	V	1
V_{IH}		V_{DD} x 0.7	V_{DD} + 0.5	V	
Timing Characteristics					

1. A 4.7k - 10kΩ pull-up resistor to V_{DD} on host is required.
2. A 10 kΩ pull-up resistor to V_{DD} is present on the transceiver.
3. See Tx_Disable on page 6 and Operation on page 9 for timing relationships.
4. See “Two-Wire Interface Capable” on page 9
5. See Operation on page 9.
6. See Rx_LOS on page 7 for timing relations.

Control Electrical Interface

Symbol	Parameter	Min	Max.	Unit	Note(s)
t_off	Tx_Disable Assert time		10	µs	3
t_on	Tx_Disable De-assert time		1	ms	3
t_reset	Tx_Disable (time to start reset)	10		µs	3
t_serial	Two-Wire Initialization Time		250	ms	4
t_init	Initialization Time		300	ms	5
t_fault	Tx_Fault Assert Time		100	µs	5
t_loss_on	Rx_LOS Assert Delay		100	µs	6
t_loss_off	Rx_LOS De-Assert Delay		100	µs	6

1. A 4.7k - 10kΩ pull-up resistor to V_{DD} on host is required.
2. A 10 kΩ pull-up resistor to V_{DD} is present on the transceiver.
3. See Tx_Disable on page 6 and Operation on page 9 for timing relationships.
4. See “Two-Wire Interface Capable” on page 9
5. See Operation on page 9.
6. See Rx_LOS on page 7 for timing relations.

Optical Receiver Specifications

Symbol	Parameter	Min	Typical	Max.	Unit	Notes
λ	Operating Wavelength	1270		1365	nm	
RL	Return Loss of Receiver	12			dB	
OMA_{op}	OMA operational range - 4.25 Gb/s	29	10	2000	µW (pk-pk)	1, 2
OMA_{op}	OMA operational range - 2.125 Gb/s	15	6	2000	µW (pk-pk)	1, 2
OMA_{op}	OMA operational range - 1.0625 Gb/s	15	6	2000	µW (pk-pk)	1, 2
P_{off}	Rx_LOS Assert Level	-30		-20	dBm (avg)	3
P_{on}	Rx_LOS De-Assert (negate) Level			-20.5	dBm (avg)	3
	Rx_LOS Hysteresis	0.5	2	5	dB (optical)	3
BW_{Rx}	Receiver Electrical 3 dB Upper Cutoff Frequency			5000	MHz	

1. The minimum and maximum values of the average received power in dBm give the input power range to maintain a BER < 10^{-12} when the data is sampled in the center of the receiver eye. These values take into account power penalties caused by the use of a laser transmitter with a worst-case combination of spectral width, extinction ratio and pulse shape characteristics.
2. Optical Modulation Amplitude (OMA) is defined as the difference in optical power between a logic level one and a logic level zero. The Optical Modulation Amplitude is defined in terms of average optical power (P_{AVG} in µW) and extinction ratio (ER) as given by $OMA=2P_{AVG}((ER-1)/(ER+1))$. The extinction ratio, defined as the ratio of the average optical power (in µW) in a logic level one to the average optical power in a logic level zero measured under fully modulated conditions in the presence of worst case reflections, must be the absolute (unit less linear) ratio and not expressed in dB. For example, the specified OMA at 4.25 Gb/s is equivalent to an average power of -17.3 dBm at an ER of 9 dB. At 1.0625 Gb/s and 2.125 Gb/s, the specified OMA is equivalent to an average power of -20.2 dBm at an ER of 9 dB. Typical values below the minimum specification indicate margin beyond the specification.
3. The Rx_LOS has hysteresis to minimize “chatter” on the output line. In principle, hysteresis alone does not guarantee chatter-free operation. The transceiver, however, presents an Rx_LOS line without chatter, where chatter is defined as a transient response having a voltage level of greater than 0.5 volts (in the case of going from the negate level to the assert level) and of any duration that can be sensed by the host logic.

Optical Transmitter Specifications

Symbol	Parameter	Min	Typical	Max.	Unit	Notes
λ_C	Spectral Center Wavelength (JSH-42L3AD3-5)	1285		1350	nm	
λ_C	Spectral Center Wavelength (JSH-42L3AD3-20)	1300		1325	nm	
$\Delta\lambda$	Spectral Width (JSH-42L3AD3-5)			2.0	nm (rms)	
$\Delta\lambda$	Spectral Width (JSH-42L3AD3-20)			0.2	nm (rms)	
SMSR	Side Mode Supression Ratio (JSH-42L3AD3-20)	30			dB	
PT	Launched Optical Power	-8.4		-1.0	dBm (avg)	1
ER	Extinction Ratio		6		dB	
T_{rise}/T_{fall}	Optical Rise/Fall Time (4.250 Gb/s)			90	ps	2
OMA	Optical Modulation Amplitude (JSH-42L3AD3-5)	190			μW (pk-pk)	3
OMA	Optical Modulation Amplitude (JSH-42L3AD3-20)	290			μW (pk-pk)	3
RIN_{12}	Relative Intensity Noise			-118	dB/Hz	4

1. Launched optical power is measured at the end of a two meter section of a singlemode fiber. The maximum and minimum of the allowed range of average transmitter power coupled into the fiber are worst case values to account for manufacturing variances, drift due to temperature variations, and aging effects. The minimum launched optical power specified assumes an infinite extinction ratio at the minimum specified OMA.
2. Optical transition time is the time interval required for the rising or falling edge of an optical pulse to transition between the 20% and 80% amplitudes relative to the logical 1 and 0 levels. This is measured through a 4th order Bessel -Thompson filter with 0.75 * Data Rate 3-dB bandwidth and corrected to the full bandwidth value. Use of the 4G FC compliance filter results in an equivalent rise/fall time specification of 116 ps.
3. Optical Modulation Amplitude (OMA) is defined as the difference in optical power between a logic level one and a logic level zero. The Optical Modulation Amplitude is defined in terms of average optical power (P_{AVG} in μW) and extinction ratio (ER) as given by $OMA=2P_{AVG}((ER-1)/(ER+1))$. In this expression, the extinction ratio, the ratio of the average optical power (in μW) in a logic level one to the average optical power in a logic level zero measured under fully modulated conditions in the presence of worst case reflections, must be the absolute (unit less linear) ratio and not expressed in dB. The specified Optical Modulation Amplitude is equivalent to an average power of -7.3 dBm at an extinction ratio of 9 dB.
4. RIN_{12} is the laser noise, integrated over a specified bandwidth, measured relative to average optical power with 12dB return loss. See ANSI Fibre Channel Specification Annex A.5.

Optical Cable and Connector Specifications

Symbol	Parameter	Min	Typical	Max.	Unit	Notes
9/125 μm Cable Specifications (Singlemode 1310nm)						
L	Length - 4.25 Gb/s (JSH-42L3AD3-5)	2		5000	m	2
L	Length - 4.25 Gb/s (JSH-42L3AD3-20)	2		20000	m	2
L	Length - 2.125 Gb/s (JSH-42L3AD3-5)	2		11000	m	2
L	Length - 2.125 Gb/s (JSH-42L3AD3-20)	2		28000	m	2
L	Length - 1.0625 Gb/s (JSH-42L3AD3-5)	2		20000	m	2
L	Length - 1.0625 Gb/s (JSH-42L3AD3-20)	2		28000	m	2
μ_c	Attenuation @ λ = 1310 nm		0.3	0.35	dB/km	
LC Optical Connector Specifications (Multimode)						
μ_{con}	Nominal Attenuation		0.2	0.4	dB	1
σ_{con}	Attenuation Standard Deviation		0.1		dB	1
	Connects/Disconnects			250	cycles	1

1. The optical interface connector dimensionally conforms to the industry standard LC type connector documented in [1]. A dual keyed LC receptacle mechanically aligns the optical transmission fiber to the SFP.
2. Distance stated is when two JDSU transceivers are used, one at each end of the link.

Electrical Connector

Symbol	Parameter	Max.	Unit
	Insertion/Removal Cycles	100	Cycles

Dust Plug / Aqueous Wash

A JDSU process/dust plug provided with the module must be in place for any dry-air cleaning processes. The module cannot be immersed in any cleaning solvents nor withstand an aqueous wash. Only the process/dust plug provided with the module is allowed. If the process/dust plug is not contaminated during non-installed use, it may be re-used.

Two-Wire Interface Timing Specifications

Parameter	Symbol	Min	Max	Units	Notes
Clock Frequency	f_{SID}		100	kHz	1
Clock Pulse Width Low	t_{LOW}	4.7		µs	1
Clock Pulse Width High	t_{HIGH}	4.0		µs	1
Clock Low to Data Out Valid	t_{AA}	0.1	4.5	µs	1
Initialization Time	t_{serial}		250	ms	3
Time the data line must be free before a new transmission can start	t_{BUF}	4.7		µs	1
Start Hold Time	$t_{HD.STA}$	4.0		µs	1
Start Set-up Time	$t_{SU.STA}$	4.7		µs	1
Data In Hold Time	$t_{HD.DAT}$	0		µs	1
Data In Set-up Time	$t_{SU.DAT}$	200		ns	1
Inputs Rise Time	t_R		1.0	µs	1
Inputs Fall Time	t_F		300	ns	1
Stop Set-up Time	$t_{SU.STO}$	4.7		µs	1
Data Out Hold Time	t_{DH}	100		ns	1
Vdd Hold Time for User Write	t_{VddH}	25+(N x 10)		ms	2

1. See Two-Wire Interface Figure 8 on page 14 for timing relationships. See Two-Wire Protocol for Serial ID and Digital Diagnostic Monitoring Information on page 11 for information on protocol.
2. The Vdd supply to the transceiver must remain valid for 25 + (N x 10) ms, where N is the number of bytes desired to write to the scratch space (bytes 128-247 in 0xA2 address). For example: A single byte write will require 35 ms of valid supply voltage after the Stop bit for that instruction is completed. A sequential multi-byte write of the entire 120 bytes into the user scratch space will require the supply to remain valid for at least 1.23 s after the stop bit is completed.
3. The time from application of 3.0 V or greater Vdd supply at the transceiver voltage inputs to when the transceiver will be capable of responding to a start sequence on the two-wire interface.

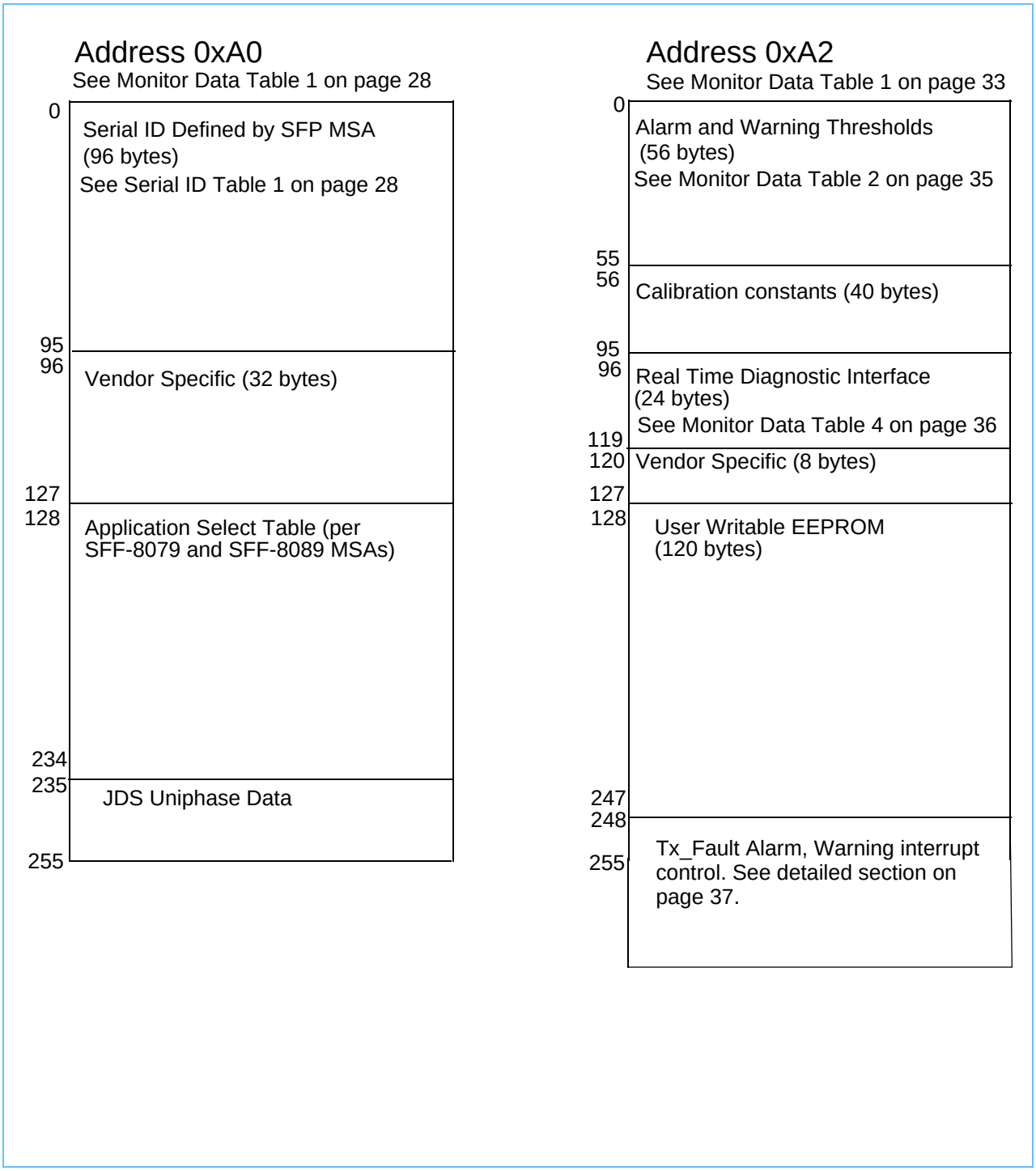
SFF 8472 Monitored Values

Parameter	Min	Max	Units	Notes
Received Optical Power Meter Dynamic Range	-20	+1.0	dBm	1
Received Optical Power Meter Accuracy	-2.0	+2.0	dB	2,3
Transmitted Optical Power Meter Dynamic Range	-9	-1.0	dBm	2
Transmitted Optical Power Meter Accuracy	-2.0	+2.0	dB	2
Laser Bias Current Meter Dynamic Range	4.0	90	mA	2
Laser Bias Current Meter Accuracy	-0.90	+0.90	mA	2
Power Supply Voltage Meter Dynamic Range	2.8	4.5	V	2
Power Supply Voltage Meter Accuracy	-0.10	0.10	V	2
Transceiver Temperature Meter Dynamic Range	-40	100	°C	2
Transceiver Temperature Meter Accuracy	-3	+3	°C	2

1. Actual optical power incident on the receiver. This range, when coupled with the accuracy specified means that the power meter can read from -18 dBm to +3 dBm when input optical power is in the range -16 dBm to +1 dBm.
2. When transceiver is operated within its specified temperature and power supply voltage dynamic operating ranges.
3. When optical input power is within the optical power meter specified dynamic operating range.

Two-Wire Interface Memory Map

Below is a summary of the transceiver memory map. The transceiver provides multiple application selection capability in accordance with SFF-8079+[6]. Modifications to the memory map in support of this feature are to be determined. Additional details can be found in the sections that follow.



Serial ID Data Descriptions (Page/Device Address 0xA0)

All ID information is stored in eight-bit parameters addressed from 0x00 to 0x7F. All numeric information fields have the lowest address in the memory space storing the highest order byte. The highest order bit is always transmitted first. All numeric fields will be padded on the left with zeros. All character strings are ordered with the first character to be displayed located in the lowest address of the memory space. All character strings will be padded on the right with ASCII spaces (0x20) to fill empty bytes.

Check Codes

The check codes contained within the identification data are one byte codes that can be used to verify that the data in previous addresses is valid. CC_BASE check code is the lower eight bits of the sum of the contents of bytes 0-62. CC_EXT check code is the lower eight bits of the sum of the contents of bytes 64-94.

Serial ID Table 1 Data Fields - Page/Device Address 0xA0

Data Address	Field Size (Bytes)	Value (Hex)	Value (Binary)	Value (ASCII)	Name of Field	Description of Field
Base ID Fields						
0	1	03	00000011		Identifier	SFP transceiver
1	1	04	00000100		Ext. Identifier	Extended identifier of type of serial transceiver
2	1	07	00000111		Connector	LC connector
3	8	00	00000000		Transceiver Codes	Reserved
4		00	00000000			SONET
5		00	00000000			SONET
6		00	00000000			No GbE Compliance
7		12	00010010			Long Distance Longwave Laser
8		0	00000000			
9		01	00000001			Singlemode fiber
10		15	00010101			4G, 2G, 1G FC
11	1	01	00000001		Encoding	8b/10b Encoding
12	1	2B	00101011		BR, nominal	Nominal bit rate in units of 100 Mb/s.
13	1	00	00000000		Reserved	
14	1	05 or 14	00000101 or 00010100	5 or 20	Fiber Length (singlemode) (km)	Link length supported for 9/125 μm fiber in units of km
15	1	32 or C8	00110010 or 11001000	50 or 200	Fiber Length (singlemode) (100m)	Link length supported for 9/125 μm fiber in units of 100 meters
16	1	00	00000000		Fiber Length (50/125μm) (10m)	Link length supported for 50/125 μm fiber in units of 10 meters
17	1	00	00000000		Fiber Length (62.5/125μm) (10m)	Link length supported for 62.5/125 μm fiber in units of 10 meters
18	1	00	00000000		Length (coppper)	Link length supported for copper in units of meters
19	1	00	00000000		Reserved	

Serial ID Table 1 Data Fields - Page/Device Address 0xA0

Data Address	Field Size (Bytes)	Value (Hex)	Value (Binary)	Value (ASCII)	Name of Field	Description of Field
20-35	16	4A		J	Vendor name	SFP transceiver vendor name (ASCII)
		44		D		
		53		S		
		20		(space)		
		55		U		
		4E		N		
		49		I		
		50		P		
		48		H		
		41		A		
		53		S		
		45		E		
		20		(space)		
		20		(space)		
		20		(space)		
		20		(space)		
36	1	00	00000000		Reserved	
37-39	3	00	00000000		Vendor OUI	SFP transceiver vendor IEEE company ID
		01	00000001			
		9C	10011100			

Serial ID Table 1 Data Fields - Page/Device Address 0xA0

Data Address	Field Size (Bytes)	Value (Hex)	Value (Binary)	Value (ASCII)	Name of Field	Description of Field
40-55	16	4A	01001010	J	Vendor Part Number	Part number provided by the SFP transceiver vendor (ASCII)
		53	01010011	S		
		48	01001000	H		
		2D	00101101	-		
		34	00110100	4		
		32	00110010	2		
		4C	01010011	L		
		33	00110101	3		
		41	01000001	A		
		44	01000010	D		
		33	00110010	3		
		2D	00101101	-		
		35	00110101	5 or 2		
		20	00100000	space, 0 or G		
		20	00100000	(space)		
		20	00100000	(space)		
56-59	4	20	00100000	(space)	Vendor revision	Revision level for part number provided by vendor (ASCII)
		20	00100000	(space)		
		20	00100000	(space)		
		20	00100000	(space)		
60-61	2	05	00000101		Wavelength	Wavelength of the laser in nm with byte 60 as MSB. (1310 nm)
		1E	00011110			
62	1	00	00000000		Reserved	
63	1				CC_BASE	Check code for Base ID Fields (addresses 0 to 62)
Extended ID Fields						
64-65	2	00	00000000		Options	Tx_Disable, Tx_Fault, Loss of Signal all implemented
		1A	00011010			
66	1	05	00000101		BR, maximum	Upper bit rate margin, units of percent (5%)
67	1	05	00000101		BR, minimum	Lower bit rate margin, units of percent (5%)
68-83	16				Vendor Serial Number	Serial number provided by the vendor (ASCII)
84-91	8				Date Code	Vendor's manufacturing date code

Serial ID Table 1 Data Fields - Page/Device Address 0xA0

Data Address	Field Size (Bytes)	Value (Hex)	Value (Binary)	Value (ASCII)	Name of Field	Description of Field
92	1	68	01101000		Digital Diagnostic Options	DDM Implemented, Internally calibrated, Rx power measurement type is average power
93	1	F0	11110000		Enhanced Options	Optional warning flags implemented, Soft Tx_Disable, Soft Tx_Fault, Soft Rx_LOS
94	1	01	00000010		SFF-8472 Compliance	Includes functionality described in Rev 9.5 SFF-9472
95	1				CC_EXT	Check code for the Extended ID Fields (addresses 64-94)
Vendor Specific ID Fields						
96-127	32			"MICRO-CODE COPY-RIGHT 2002 JDSU"	Read Only	Vendor specific data, read only

Application Select Tables

The Application Select Tables contain information that allows the host system to control internal settings which configure the transceiver for optimal perfromance at a given data rate.

The different application codes are selected via byte 111 in the A2 page. To select one of the application codes, bit 7 in byte 111 is set to 1 and bit 5:0 are set to the desired application table. The contents of the Application codes are compliant to the Application_Select MSAs SFF-8079 and SFF-8089.

Application Select Table

Byte Address	Length (bytes)	Name of Field	Description
128	1	CC_APPS	Check code for the Application Select Table. The check code is the low order 8 bits of the sum of the contents of all the bytes from byte 129 to byte 255.
129	bits (7:6)	Reserved	
129	bits (5:0)	AST Table Length, TL	A 6-bit binary number, TL, that specifies how many application table entries are defined in bytes 130 - 255 addresses. TL is valid between 0 (one entry) and 51 (for a total of 52 entries).
130	2	Application Code 0	
132	2	Application Code 1	
134	2	Application Code 2	
232	2	Application Code 52	

JDSU Transceiver Data

Data Addresses	Field Size (Bytes)	Name of FIelds	Description
235	4		
239	4		
243	4		
247	4		
251	4		

Digital Diagnostic Monitor Data Descriptions (Page/Device Address 0xA2)

The Monitor Data ID tables that follow describe the data contained in the 256 bytes of Page/Device Address 0xA2. Monitor Data Table 1 is a summary of all of the data fields in the Monitor Data section of the memory. Monitor Data Table 2 on page 34 and Monitor Data Table 4 on page 35 provide more detailed translations of data words for some of the data fields.

To guarantee coherency of the diagnostic monitoring data, the host is required to retrieve any multi-byte fields from the diagnostic monitoring data structure by the use of a single multi-byte read sequence across the

serial interface.

Monitor Data Table 1 Data Fields Summary- Page/Device Address 0xA2

Byte Address	Length (Bytes)	Description of Fields
0-55	56	Manufacturer's preset alarm and warning threshold levels.
56-95	40	Polynomial constants for externally processing raw A/D digital values. (default to Zero for Internally Calibrated parts, Serial ID Byte 92, Bit 5 set to one)
96-119	24	Real time diagnostic data, alarms, warnings and soft control bits.
120-127	8	Vendor specific.
128-247	120	User writable non-volatile scratch space.
248-255	8	Tx_Fault Alarm/Warning Interrupt Contol Bits

Internal Calibration

This transceiver contains internally calibrated values such that the values should be interpreted as follows:

Temperature: The temperature data is the internal transceiver temperature. The temperature is represented as a 16-bit signed twos complement value in increments of 1/256 °C. This yields a value from -128 to +128 °C but is only valid if within the operating specifications of the transceiver. Temperature accuracy is +/- 3 °C.

Voltage: The voltage data will be calibrated to the internally measured Transmit V_{DD} supply. The voltage is represented as a 16-bit unsigned integer with the voltage equal to the full 16-bit decimal value (0 to 65535)*100 μV. This yields a total range of 0 to 6.55 volts but is only valid if within the operating specifications of the transceiver. Accuracy is +/-3% of nominal voltage (3.3 +/- 0.10 V)

TX Bias: The TX Bias data is calibrated to reflect the average current biasing the laser diode. The TX Bias is represented as a 16-bit unsigned integer with the current value equal to the full 16-bit decimal value (0 to 65535)*2 μA. This yields a total range of 0 to 131mA but is only valid if within the operating specifications of the transceiver. Accuracy is +/-10% of nominal value over specified operating temperature and voltage.

TX Power: The TX Power data is calibrated to reflect the average power coupled into a nominal fiber [7]. The accuracy takes into account the fiber to fiber variation and also calibration test equipment accuracies. The TX Power is represented as a 16-bit unsigned integer with the power value equal to the full 16-bit decimal value (0 to 65535)*0.1 μW. This yields a total range of 0 to 6.55 mW but is only valid if within the operating specifications of the transceiver. Data is not valid when the transmitter is disabled. Accuracy is +/-2 dB over specified operating voltage and temperature.

RX Power: RX Power data is calibrated to reflect the average optical power exiting the ferrule of a nominal fiber[7]. The accuracy takes into account the fiber to fiber variation and also calibration test equipment accuracies. The RX Power is represented as a 16-bit unsigned integer with the power value equal to the full 16-bit decimal value (0 to 65535)*0.1 μW. This yields a total range of 0 to 6.55 mW but is only valid if within the operating specifications of the transceiver. Accuracy is +/- 2dB over specified operating voltage and temperature.

Digital Diagnostic Monitor Data Offsets

The Digital Diagnostic Monitor Data page is a single 256-byte page with regard to read and write access offsets. There are no mini-page sections within the 256-byte space. Contiguous, sequential accesses, without modifying the offset, will cycle through offsets 0 to 255 then return to offset 0.

Digital Diagnostic Monitor Data Write Access

The Digital Diagnostic Monitor Data page contains an area defined as a user writable, non-volatile scratch space, that can be written to by the user, and which will be non-volatile across power cycles and resets. This space can be accessed sequentially and contiguously within the offsets defined for it (refer to Monitor Data Table 1 on page 32). If during the course of a sequential, multi-byte write, the offset being written reaches the end of the user writable space, the next byte of data will be a write attempt to the vendor specific area.

Monitor Data Table 2 Alarm and Warning Threshold Levels

Byte Address	Length (Bytes)	Name	Byte Alignment	Factory Programmed Value In Units Specified by SFF-8472 Standard	Factory Programmed Equivalent Value	
0-1	2	Temp High Alarm	MSB at low address	0x5F00	95	
2-3	2	Temp Low Alarm	MSB at low address	0xDD00	-35	
4-5	2	Temp High Warning	MSB at low address	0x5A00	90	
6-7	2	Temp Low Warning	MSB at low address	0xE200	-30	
8-9	2	Voltage High Alarm	MSB at low address	0x8DCC	3.63 V	
10-11	2	Voltage Low Alarm	MSB at low address	0x7404	2.97 V	
12-13	2	Voltage High Warning	MSB at low address	0x8BD8	3.58 V	
14-15	2	Voltage Low Warning	MSB at low address	0x75F8	3.02 V	
16-17	2	Bias High Alarm	MSB at low address	0xA604	85.0 mA	
18-19	2	Bias Low Alarm	MSB at low address	0x0BB8	6.0 mA	
20-21	2	Bias High Warning	MSB at low address	0x9C40	80.0 mA	
22-23	2	Bias Low Warning	MSB at low address	0x0FA0	8.0 mA	
24-25	2	TX Power High Alarm	MSB at low address	0x1F07	0.7943 mW	-1 dBm
26-27	2	TX Power Low Alarm	MSB at low address	0x0630	0.1585 mW	-8.0 dBm
28-29	2	TX Power High Warning	MSB at low address	0x1BA7	0.7080 mW	-1.5 dBm
30-31	2	TX Power Low Warning	MSB at low address	0x07CB	0.1995 mW	-7.0 dBm
32-33	2	RX Power High Alarm	MSB at low address	0x1F07	0.7943 mW	-1.0 dBm
34-35	2	RX Power Low Alarm	MSB at low address	0x009E	0.0158 mW	-18.0 dBm
36-37	2	RX Power High Warning	MSB at low address	0x1BA8	0.7080 mW	-1.5 dBm
38-39	2	RX Power Low Warning	MSB at low address	0x00C7	0.0199 mW	-17 dBm
40-55	16	Reserved	.			

Monitor Data Table 3 Digital Diagnostic Check Sum Byte.

Byte Address	Length (Bytes)	Name	Description of Fields
95	1	Checksum	The lower eight bits of the sum of the contents of bytes 0-94.

Monitor Data Table 4 Diagnostic Data Values, Alarms, Warnings and Status Bits

Byte Address	Bit	Name	Description of Fields
96-97	All	Temperature Value[1]	Internal Transceiver Temperature (MSB at low address)
98-99	All	Voltage Value[1]	TX VDD Voltage (MSB at low address)
100-101	All	TX Bias Value[1]	Laser Diode Average Current (MSB at low address)
102-103	All	TX Power Value[1]	Average Fiber Coupled Power (MSB at low address)
104-105	All	RX Power Value[1]	Average Received Power (MSB at low address)
106-109	All	Reserved	Reserved for future MSA monitored parameters.
110	7	TX Disable State	State of TX Disable input pin
110	6	Soft TX Disable	Read/Write bit that allows software disable of laser. Writing a '1' disables the laser. Default power value is '0'. This bit is internally OR'ed with the hard TX_DISABLE pin value.
110	5	AS1 State	Digital state of AS1 input pin.
110	4	RX Rate Select AS0 State	Digital state of rate_select input pin.
110	3	Soft Rate Select	Not Applicable
110	2	TX Fault	State of TX Fault output pin.
110	1	LOS	Sate of LOS output pin.
110	0	Data Ready Bar[1,2]	Indicates transceiver has achieved power and Digital Diagnostic data is ready to be read.
111	7:6	Control Mode	Not Applicable
111	5:0	Table Select (TS)	For soft application_select, a 6-bit binary number (TS) that represents the sequence of the Application code in the AST. It is written by the host for select module behavior.
112	7	Temp High Alarm [1,3]	Set when internal temperature exceeds the bytes 0-1 level.
112	6	Temp Low Alarm [1,3]	Set when internal temperature is below the bytes 2-3 level.
112	5	Voltage High Alarm [1,3]	Set when TX VDD exceeds the bytes 8-9 level.
112	4	Voltage Low Alarm [1,3]	Set when TX VDD is below the bytes 10-11 level.
112	3	TX Bias High Alarm [1,3]	Set when Laser Diode Current exceeds the bytes 16-17 level.

1. The Digital Diagnostic Monitoring values and Alarm/Warning indicators will be set to zero, and Data Ready Bar will be set high, for certain failure mechanisms within the transceiver that do not affect the link capability of the transceiver. Refer to Vendor Specific Digital Diagnostic Monitor TX_FAULT Alarm/Warning Interrupt on page 37 for additional information on transceiver Digital Diagnostic Monitoring status.
2. The data ready bar bit is held high during module power up and prior to the first transceiver sampling of the monitored values. The bit will be set low after each first successful sampling occurs and remain low until the transceiver looses power or a failure occurs. The bit must be set low within 1 second of reaching a valid stable power supply level.
3. Bytes 112-119 contain a set of non-latched alarm and warning flags. Users can choose to read these values and use them to analyze the status of the transceiver as an alternative to decoding the real-time values in bytes 96-105. Alarm flags indicate levels that are likely to be associated with link failures. Warning flags indicate levels that are outside of normal levels, but not necessarily cause for immediate concern (could be used for end-of-life indicators).
4. The Vendor Specific area is further defined below in Vendor Specific Digital Diagnostic Monitor TX_FAULT Alarm/Warning Interrupt on page 37.

Monitor Data Table 4 Diagnostic Data Values, Alarms, Warnings and Status Bits

Byte Address	Bit	Name	Description of Fields
112	2	TX Bias Low Alarm [1,3]	Set when Laser Diode Current is below the bytes 18-19 level.
112	1	TX Power High Alarm [1,3]	Set when Avg. Fiber Coupled Power exceeds the bytes 24-25 level.
112	0	TX Power Low Alarm [1,3]	Set when Avg. Fiber Coupled Power is below the bytes 26-27 level.
113	7	RX Power High Alarm [1,3]	Set when Avg. Received Power exceeds the bytes 32-33 level.
113	6	RX Power Low Alarm [1,3]	Set when Avg. Received Power is below the bytes 34-35 level.
113	5-0	Reserved	Reserved
114-115	All	Reserved	Reserved
116	7	Temp High Warning [1,3]	Set when internal temperature exceeds the bytes 4-5 level.
116	6	Temp Low Warning[1, 3]	Set when internal temperature is below the bytes 6-7 level.
116	5	Voltage High Warning [1,3]	Set when TX VDD exceeds the bytes 12-13 level.
116	4	Voltage Low Warning [1,3]	Set when TX VDD is below the bytes 14-15 level.
116	3	TX Bias High Warning [1,3]	Set when Laser Diode Current exceeds the bytes 20-21 level.
116	2	TX Bias Low Warning [1,3]	Set when Laser Diode Current is below the bytes 22-23 level.
116	1	TX Power High Warning[1, 3]	Set when Avg. Fiber Coupled Power exceeds the bytes 28-29 level.
116	0	TX Power Low Warning [1,3]	Set when Avg. Fiber Coupled Power is below the bytes 30-31 level.
117	7	RX Power High Warning [1,3]	Set when Avg. Received Power exceeds the bytes 36-37 level.
117	6	RX Power Low Warning [1,3]	Set when Avg. Received Power is below the bytes 38-39 level.
117	5-0	Reserved	Reserved
118-119	All	Reserved	Reserved
120-127	All	Vendor Specific [4]	Vendor Specific

1. The Digital Diagnostic Monitoring values and Alarm/Warning indicators will be set to zero, and Data Ready Bar will be set high, for certain failure mechanisms within the transceiver that do not affect the link capability of the transceiver. Refer to Vendor Specific Digital Diagnostic Monitor TX_FAULT Alarm/Warning Interrupt on page 37 for additional information on transceiver Digital Diagnostic Monitoring status.
2. The data ready bar bit is held high during module power up and prior to the first transceiver sampling of the monitored values. The bit will be set low after each first successful sampling occurs and remain low until the transceiver looses power or a failure occurs. The bit must be set low within 1 second of reaching a valid stable power supply level.
3. Bytes 112-119 contain a set of non-latched alarm and warning flags. Users can choose to read these values and use them to analyze the status of the transceiver as an alternative to decoding the real-time values in bytes 96-105. Alarm flags indicate levels that are likely to be associated with link failures. Warning flags indicate levels that are outside of normal levels, but not necessarily cause for immediate concern (could be used for end-of-life indicators).
4. The Vendor Specific area is further defined below in Vendor Specific Digital Diagnostic Monitor TX_FAULT Alarm/Warning Interrupt on page 37.

Vendor Specific Digital Diagnostic Monitor TX_FAULT Alarm/Warning Interrupt

The transceiver has the ability to be programmed to indicate TX_FAULT when one of the five DDM signals goes outside an alarm or warning threshold. This allows the customer the option of using the TX_FAULT as an interrupt instead of constantly polling the diagnostic signals. The TX_FAULT Alarm/Warning interrupt control bytes are accessible as one of the selectable tables in the Vendor specific area at offset 248-255.

To enable the TX_FAULT as an Alarm/Warning, use the following procedure:

This alarm/warning interrupt enable/latch space will be volatile across power-cycles and resets. This space can be accessed sequentially and contiguously within the offsets defined for it. If during the course of a sequential, multi-byte write, the offset being written reaches the end of this vendor specific area, the next byte of data that will be attempted to be written will be at offset 0.

The Alarm/Warning Interrupt Enable bits are written by the host. They are used by the transceiver to generate a TX_FAULT signal usable as an interrupt to the host for an alarm/warning condition. The general definition of the function is that when the host sets an Interrupt Enable bit (offsets 248-251) for an Alarm/Warning to 0b1, then the corresponding Alarm/Warning Latch bit (offsets 252-255) will be latched to 0b1 when the corresponding Alarm/Warning bit (Alarm bits at offsets 112-113 and Warning bits at offsets 116-117) becomes active. The Alarm/Warning Latch bit will remain 0b1 until the host clears the Latch bit by writing a 0b1 to it, at which time the transceiver will re-process the Latch bit. While any of the Alarm/Warning Latch bits are a 0b1, the transceiver will set the TX_FAULT signal active.

Note: When used in the Alarm/Warning Interrupt mode, the TX_FAULT signal does not necessarily indicate that the transceiver is not transmitting. When TX_FAULT becomes active, the host should disable all Alarm/Warning Interrupt Enable bits and clear all Alarm/Warning Latch bits In order to determine whether there is a hardware TX_FAULT that does indicate hardware transmission loss.

Monitor Data Table 9 Alarm/Warning Enables and Latches

Byte Address	Bit	Name	Description of Fields
248	7	Temp High Alarm Interrupt Enable [1]	Enable bit for the temperature high alarm.
248	6	Temp Low Alarm Interrupt Enable [1]	Enable bit for the temperature low alarm.
248	5	Voltage High Alarm Interrupt Enable [1]	Enable bit for the voltage high alarm.
248	4	Voltage Low Alarm Interrupt Enable [1]	Enable bit for the voltage low alarm.
248	3	TX Bias High Alarm Interrupt Enable [1]	Enable bit for the laser current high alarm.
248	2	TX Bias Low Alarm Interrupt Enable [1]	Enable bit for the laser current low alarm.
248	1	TX Power High Alarm Interrupt Enable [1]	Enable bit for the fiber coupled power high alarm.
248	0	TX Power Low Alarm Interrupt Enable [1]	Enable bit for the fiber coupled power low alarm.
249	7	RX Power High Alarm Interrupt Enable [1]	Enable bit for the received power high alarm.
249	6	RX Power Low Alarm Interrupt Enable [1]	Enable bit for the received power low alarm.
249	5-0	Reserved	Reserved
250	7	Temp High Warning Interrupt Enable [1]	Enable bit for the temperature high warning.

Byte Address	Bit	Name	Description of Fields
250	6	Temp Low Warning Interrupt Enable [1]	Enable bit for the temperature low warning.
250	5	Voltage High Warning Interrupt Enable [1]	Enable bit for the voltage high warning.
250	4	Voltage Low Warning Interrupt Enable [1]	Enable bit for the voltage low warning.
250	3	TX Bias High Warning Interrupt Enable [1]	Enable bit for the laser current high warning.
250	2	TX Bias Low Warning Interrupt Enable [1]	Enable bit for the laser current low warning.
250	1	TX Power High Warning Interrupt Enable [1]	Enable bit for the fiber coupled power high warning.
250	0	TX Power Low Warning Interrupt Enable [1]	Enable bit for the fiber coupled power low warning.
251	7	RX Power High Warning Interrupt Enable [1]	Enable bit for the received power high warning.
251	6	RX Power Low Warning Interrupt Enable [1]	Enable bit for the received power low warning.
251	5-0	Reserved	Reserved
252	7	Temp High Alarm Latch [2]	Latched bit for the temperature high alarm.
252	6	Temp Low Alarm Latch [2]	Latched bit for the temperature low alarm.
252	5	Voltage High Alarm Latch [2]	Latched bit for the voltage high alarm.
252	4	Voltage Low Alarm Latch [2]	Latched bit for the voltage low alarm.
252	3	TX Bias High Alarm Latch [2]	Latched bit for the laser current high alarm.
252	2	TX Bias Low Alarm Latch [2]	Latched bit for the laser current low alarm.
252	1	TX Power High Alarm Latch [2]	Latched bit for the fiber coupled power high alarm.
252	0	TX Power Low Alarm Latch [2]	Latched bit for the fiber coupled power low alarm.
253	7	RX Power High Alarm Latch [2]	Latched bit for the received power high alarm.
253	6	RX Power Low Alarm Latch [2]	Latched bit for the received power low alarm.
253	5-0	Reserved	Reserved
254	7	Temp High Warning Latch [2]	Latched bit for the temperature high warning.
254	6	Temp Low Warning Latch [2]	Latched bit for the temperature low warning.
254	5	Voltage High Warning Latch [2]	Latched bit for the voltage high warning.
254	4	Voltage Low Warning Latch [2]	Latched bit for the voltage low warning.
254	3	TX Bias High Warning Latch [2]	Latched bit for the laser current high warning.
254	2	TX Bias Low Warning Latch [2]	Latched bit for the laser current low warning.
254	1	TX Power High Warning Latch [2]	Latched bit for the fiber coupled power high warning.
254	0	TX Power Low Warning Latch [2]	Latched bit for the fiber coupled power low warning.
255	7	RX Power High Warning Latch [2]	Latched bit for the received power high warning.
255	6	RX Power Low Warning Latch [2]	Latched bit for the received power low warning.
255	5-0	Reserved	Reserved

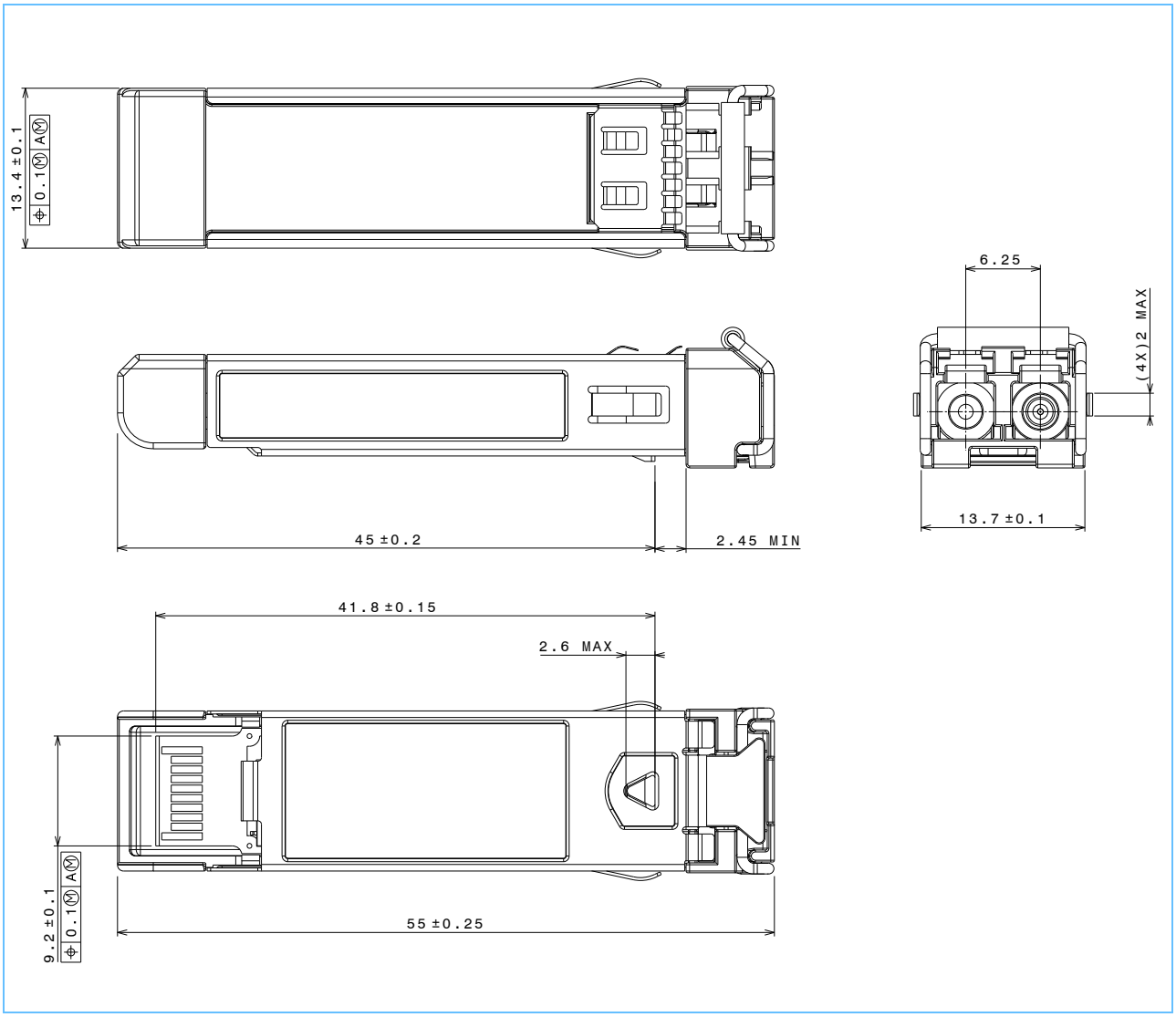
Byte Address	Bit	Name	Description of Fields

1. The alarm/warning interrupt enable bits are writable by the host to either 0b0 or 0b1. Their default value after a reset is 0b0. To enable multiple bits, the host must write the byte at the appropriate offset with a value that is an OR of all bits that are to be set to the interrupt enabled state.
2. The alarm/warning latch bits are only set to 0b1 by the transceiver, but can be cleared to 0b0 by the host writing a 0b1 to the appropriate bit position. Only those bits that are written to 0b1 will be cleared. Upon clearing a bit, the transceiver will re-process the Latch bit, and if the corresponding alarm/warning bit is still active, and the corresponding interrupt enable bit is still set to 0b1, the Latch bit will remain set to 0b1, thus causing TX_FAULT to remain active.

Mechanical Description

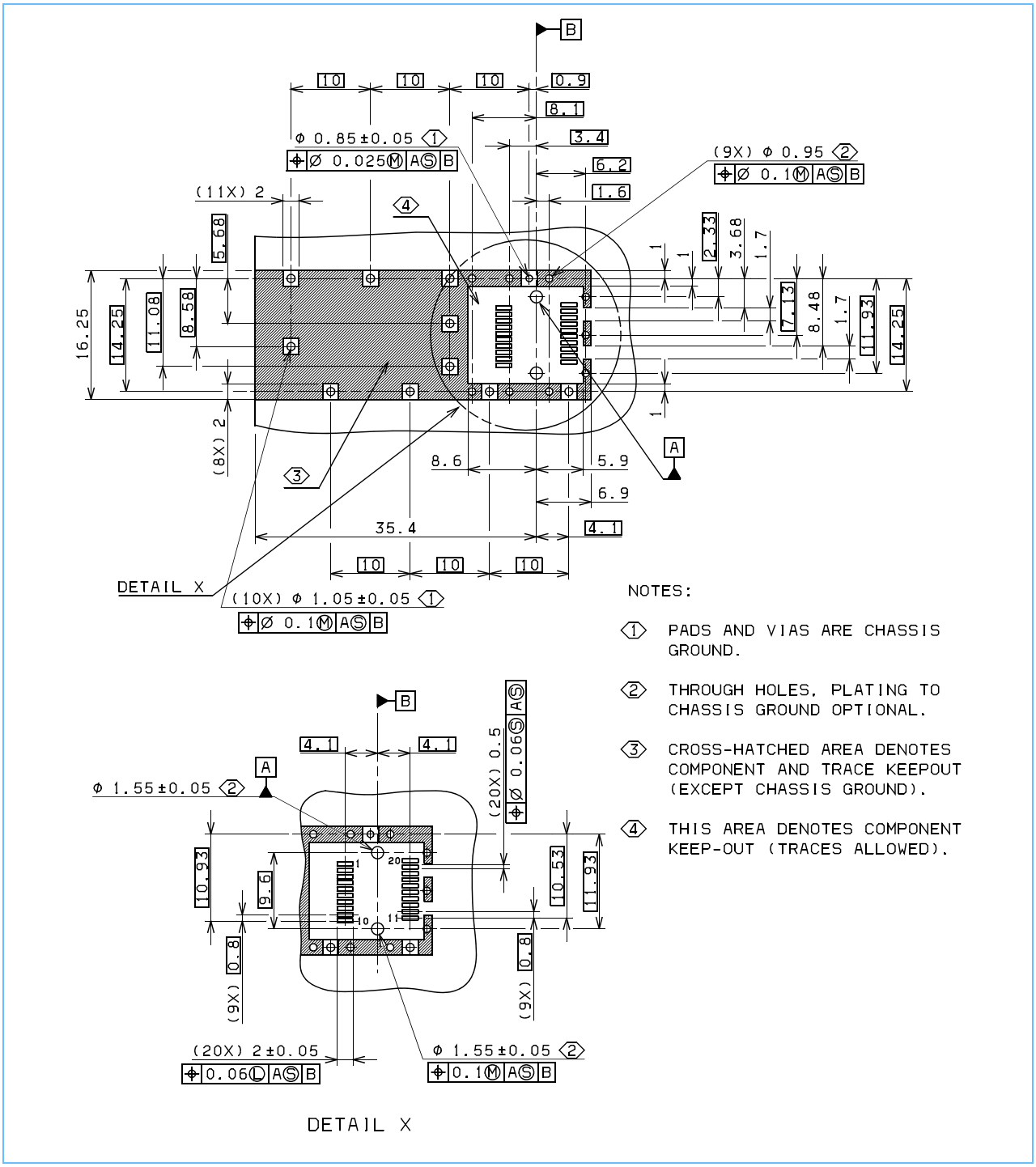
Package Diagram

Units are in millimeters.



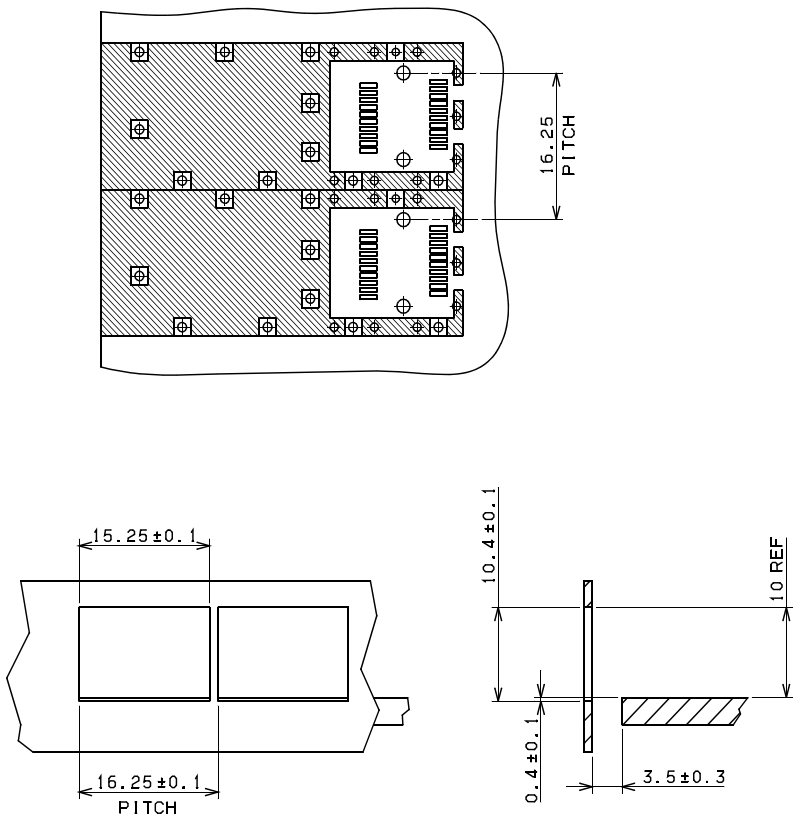
Host Card Footprint (Page 1 of 2)

Units are in millimeters.

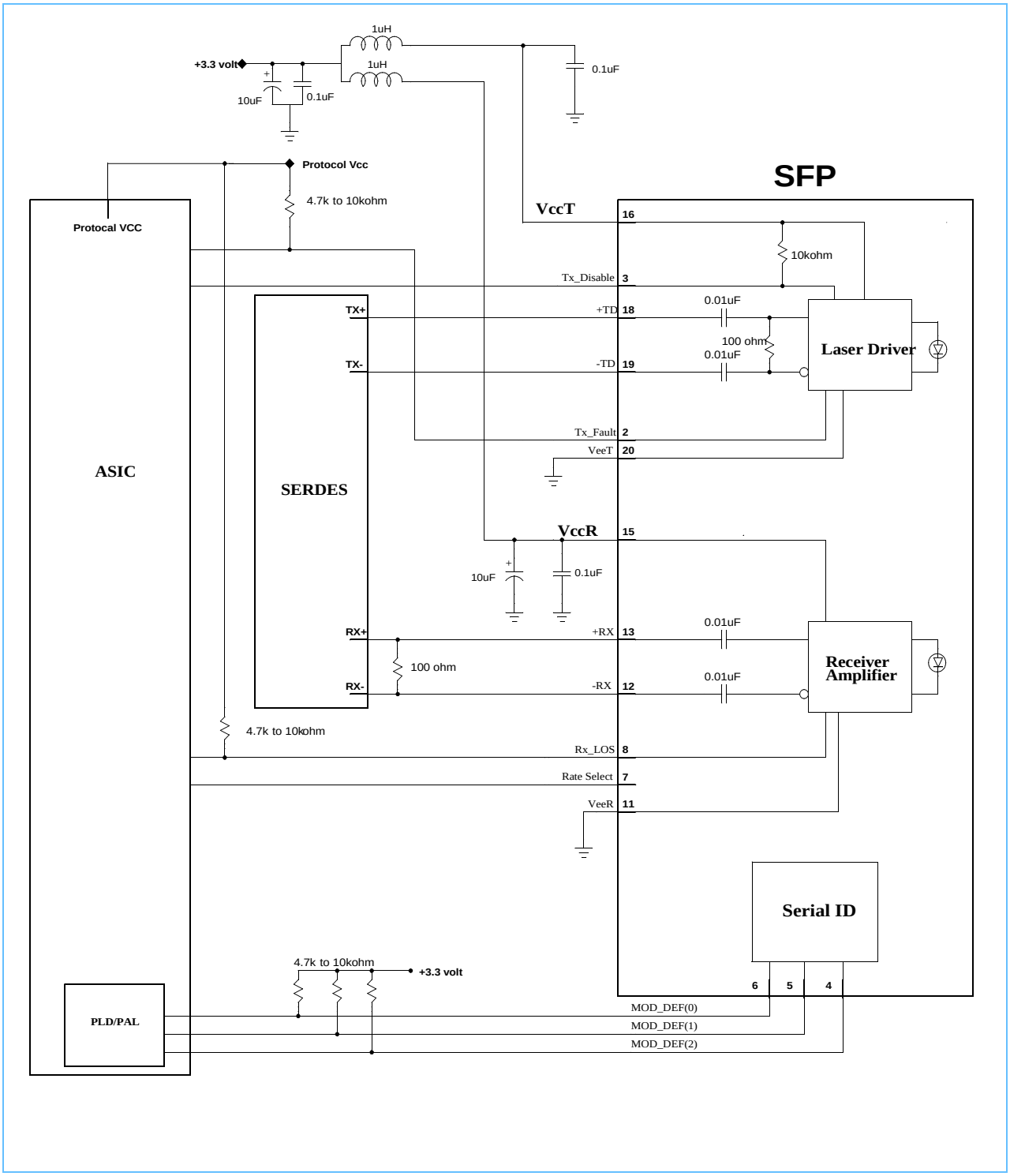


Host Card Footprint (Page 2 of 2)

Units are in millimeters.



Suggested Transceiver/Host Interface



References

Standards

1. American National Standards Institute Inc. (ANSI), T11/Project 1235-DT/Rev 13, Fibre Channel-Physical Interface (FC-PI-2 rev. 7). Drafts of this standard are available to members of the standards working committee. For further information see the T11.2 website at www.t11.org.
2. American National Standards Institute Inc. (ANSI), T11.2/Project 1230/Rev10, Fibre Channel-Methodologies for Jitter Specifications (MJS). Drafts of this standard are available to members of the standards working committee. For further information see the T11.2 website at www.t11.org.

Industry Specifications

3. A.X. Widmer and P.A. Franaszek, “A DC-Balanced, Partitioned-Block, 8B/10B Transmission Code,” *IBM Journal of Research and Development*, vol. 27, no. 5, pp. 440-451, September 1983. This paper fully defines the 8B/10B code. It is primarily theoretical.
4. A.X. Widmer, The ANSI Fibre Channel Transmission Code, *IBM Research Report, RC 18855 (82405)*, April, 23 1993. Copies may be requested from:

   Publications
   IBM Thomas J. Watson Research Center
   Post Office Box 218
   Yorktown Heights, New York 10598
   Phone: (914) 945-1259
   Fax: (914) 945-4144
5. SFF Document Number: SFF-8472, revision 9.4 “Digital Diagnostic Monitoring Interface for Optical Transceivers,” August 1, 2002. This document defines features of the 512 bytes of RAM space accessible by the two-wire interface.
6. SFF Document Number: SFF-8079+, Revision 1.1, “SFP Form Factor (Small Form Factor Pluggable) Rate Select Functionality and Multiple Application Selection Capability”, November 19,2003.

Production Notes

7. The fiber type used for the calibration of Tx and Rx power monitoring functions is a singlemode fiber.

All statements, technical information and recommendations related to the products herein are based upon information believed to be reliable or accurate. However, the accuracy or completeness thereof is not guaranteed, and no responsibility is assumed for any inaccuracies. The user assumes all risks and liability whatsoever in connection with the use of a product or its application. JDSU reserves the right to change at any time without notice the design, specifications, function, fit or form of its products described herein, including withdrawal at any time of a product offered for sale herein. JDSU makes no representations that the products herein are free from any intellectual property claims of others. Please contact JDSU for more information. JDSU and the JDSU logo are trademarks of JDS Uniphase Corporation. Other trademarks are the property of their respective holders.

The SFP module described herein contains microcode which is The purchaser is granted a limited license to use the microcode for the purposes described in this specification. The microcode remains the property of JDSU and may not be decoded, reverse compiled, altered, extracted from the module storage device, copied, redistributed, or reused without the express written consent of JDSU.